Claims

[c1] What is claimed is:

1.A test circuit comprising:

a substrate;

a first deep trench polysilicon layer formed in the substrate;

a first top-thin oxide layer disposed over the first deep trench polysilicon layer;

a second deep trench polysilicon layer laterally formed in the substrate on one side of the first deep trench polysilicon layer;

a second top-thin oxide layer disposed over the second deep trench polysilicon layer;

a shallow trench isolation embedded in the substrate and located between the first deep trench polysilicon layer and the second deep trench polysilicon layer; and

a word line laid on the substrate, the word line partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer;

an ion well implanted in the substrate and being electrically connected with the first deep trench polysilicon layer; and

a contact electrically connecting the ion well and a bit line for supplying the first deep trench polysilicon layer with a pre-selected voltage.

[c2] 2.The test circuit of claim 1 wherein the first deep trench polysilicon layer is located at one side of the word line and the second deep trench polysilicon layer is located at the other side of the word line.

[c3] 3.The test circuit of claim 1 wherein both of thickness of the first top-thin oxide layer and thickness of the second top-thin oxide layer are smaller than a thickness of the shallow trench isolation.

[c4] 4.The test circuit of claim 1 wherein the shallow trench isolation is formed by performing a shallow trench isolation (STI) process.

[c5] 5.The test circuit of claim 1 wherein the first top-thin oxide layer, the second top-thin oxide layer, and the shallow trench isolationr are composed of silicon dioxide.

[c6] 6.The test circuit of claim 5 wherein the first top-thin oxide layer, the second top-thin oxide layer, and the shallow trench isolationr are composed of CVD silicon dioxide.

[c7] 7.The test circuit of claim 1 wherein the ion well does not overlap with any word line.

[c8] 8.The test circuit of claim 1 wherein the word line is composed of polysilicon.

[c9] 9.A test key for evaluating isolation quality of a top-thin oxide layer of deep trench DRAM cells, comprising:
a substrate;
a first deep trench capacitor formed in the substrate;
a first top-thin oxide layer disposed over the first deep trench capacitor;
a second deep trench capacitor formed in the substrate and being electrically connected with the first deep trench capacitor;
a second top-thin oxide layer disposed over the second deep trench capacitor;
a shallow trench isolation embedded in the substrate for isolating the first deep trench capacitor from the second deep trench capacitor;
a first word line formed on the substrate partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer;
an ion well implanted in the substrate and being electrically connected with the first deep trench capacitor; and
a contact electrically connecting the ion well and a bit line for supplying the first deep trench capacitor with a pre-selected voltage;
wherein the second deep trench capacitor is electrically connected with the first deep trench capacitor through a connecting region.

[c10] 10.The test key of claim 9 wherein the connecting region comprises a third deep trench capacitor and the shallow trench isolation covers the third deep trench capacitor.

[c11] 11.The test key of claim 9 wherein the first deep trench capacitor comprises a polysilicon layer located underneath the first top-thin oxide layer.

[c12] 12.The test key of claim 11 wherein the polysilicon layer is electrically

connected with the ion well through a diffusion region.

[c13] 13.The test key of claim 9 further comprising a second word line laid on the substrate on at side of the first word line and the second word line partially covers the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer.

[c14] 14.The test key of claim 13 wherein the first and second word lines are composed of polysilicon.

[c15] 15.A test key comprising:
a substrate;
a deep trench capacitor formed in the substrate;
at least one active region defined on the substrate, wherein the active region comprises a first region, a second region and an ion well;
a thermal oxide layer formed in the first region;
a top-thin oxide layer formed in the second region, wherein the second region overlaps with the deep trench capacitor; and
at least one word line partially overlapping with the top-thin oxide layer;
wherein the ion well is electrically connected with a polysilicon electrode of the deep trench capacitor and the thermal oxide layer within the first region does not overlap with any word line.